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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,332	01/13/2004	Matthew S. Taubman	50005-172	3464

30565 7590 03/15/2005

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,332	TAUBMAN, MATTHEW S.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28 and 30-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 1/24/2005. Claims 28 and 30-46 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 28, 30-31, 33-36, 38 and 40-45 are rejected under 35 U.S.C. 102(b) as being anticipated by Dowd et al. (USP 5,123,024), prior art of record. Figure 1 of Dowd et al. shows a circuit having a transistor (14) operating in common base (column 2, lines 54), two input signal pathways (Id at node 5; Idac to node 5) coupled to a first terminal (emitter 16) of the transistor, providing a virtual ground at the first terminal of the transistor device (at high frequency the feedback capacitor 12 is shorted, the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded), providing an output from the second terminal of the transistor device to a current dependent load (30, 32) as called for in claims 28, 35 and 42-43.

Regarding claim 30, controlling the transistor with a servo device (7), providing feedback to the servo device from the first terminal of the transistor.

Regarding claims 31, 38 and 44, the negative feedback is coupled to the negative input of the differential amplifier 8, the positive input of the differential amplifier is coupled to ground.

Regarding claims 33, 36 and 40, diode 32 is laser diode, the control voltage is the output of the diode 10, sweep voltage is the output of the resistor 6, control signal generator (4).

Regarding claims 34 and 45, a constant bias current is seen as current source 22, a second current source is the resistor 28 biased by the supply voltage +V.

Regarding claim 41, first current source (the resistor 16 being biased by the voltage -V), second current source (22).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dowd et al. (USP 5,123,024),prior art cited on the PTOL-1449. Figure 1 of Dowd et al. shows a circuit having a transistor (14) operating in common base (column 2, lines 54), two input signal pathways (Id at node 5; Idac to node 5) coupled to a first terminal (emitter 16) of the transistor, providing a virtual ground at the first terminal of the transistor device (at high frequency the feedback capacitor 12 is shorted, the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded), providing an output from the second terminal of the transistor device to a current dependent load (30, 32).

The differences seen between Dowd et al. and the present invention is that the present invention calls for quantum cascade laser configuration. However, it is known in the art quantum cascade laser configuration is a variation of a laser diode. The substitution of one for the other will not alter the overall performance of the circuit. Therefore, outside of non-obvious

results, the obviousness of using quantum cascade laser configuration over a laser diode will not be patentable under 35USC 103(a).

3. Claims 32, 39 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowd et al. (USP 5,123,024), prior art cited on the PTOL-1449, in view of Prentice (USP 6,344,762), newly cited prior art. Figure 1 of Dowd et al. shows a circuit having a transistor (14) operating in common base (column 2, lines 54), two input signal pathways (Id at node 5; Idac to node 5) coupled to a first terminal (emitter 16) of the transistor, providing a virtual ground at the first terminal of the transistor device (at high frequency the feedback capacitor 12 is shorted, the first terminal of the transistor is at virtual ground because the positive terminal of the differential amplifier is grounded), providing an output from the second terminal of the transistor device to a current dependent load (30, 32).

Figure 1 of Dowd et al. does not show a different transistor being coupled to the base of the transistor and the different transistor including ground coupled emitter as called for in claims 32, 39 and 46. Figure 1 of Prentice shows the detailed structures of a differential amplifier having emitter coupled to ground. Prentice's differential amplifier is simply having only two transistors and two resistors thus saving space on a chip and minimize power consumption. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to use Prentice's differential amplifier in place of Dowd et al.'s differential amplifier (8) for the purpose of saving space and reduce power consumption.

Response to Arguments

4. Applicant's arguments filed 1/24/2005 have been fully considered but they are not persuasive. Applicant argues that Dowd et al. does not teach providing a virtual ground at the

first terminal of the transistor device is not persuasive. At high frequency the feedback capacitor 12 of figure 1 become shorted, thus providing a virtual ground at the first terminal (emitter terminal) of the transistor device 14. Therefore, the limitations of claims 28, 30-31. 33-34 and 42-45 are fully met.

5. Regarding claim 35, applicant argues that Dowd et al. fails to teach to maintain emitter of the transistor device at a predefined voltage" is not persuasive. At high frequency the feedback capacitor 12 of figure 1 become shorted, thus the differential amplifier 8 operates to maintain the emitter of the transistor 14 at a predefined voltage (ground potential). Therefore, the limitations of claims 35, 36, 38 and 40-41 are fully met.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

3/11/2005